Department of Electronics & Telecommunication Engineering

To,
IQAC,
Jaihind College of Engineering,
Kuran-410 511

Subject: Sanction to organize the following Events in the month of March Academic Year 2023-24.

Respected Sir/Madam,

With reference to the above-mentioned subject, the Department of Electronics & Telecommunication Engineering plans to organize seminar on VLSI to 29/02/2024 with the following details.

Sr. No	Name of Event	Level (State/National/intern.)	No. of Days/ Hrs.	Date of Conduction	Approx. Participants	Approximate Expenditure	Collaborative Agency / MoU / Organization	Name of Resource Person
1	*Seminar on VLSI*	-	*01*	*29 Feb 2024*	*74*	-	*Maven Silicon*	*Christopher*

Kindly accept the same and do the needful. Thank You.

Name & Sign of Event Coordinator

Name and Sign of Head of Department

Head of Department (E & TC) Jaihind College of Engineering, Tal-Junnar, Dist. Pune

For IQAC Only

Date of Meeting:

Remark:

IQAC

Director
Internal Quality Assurance Cell
Jaihind College of Engineering,Kuran
Tal.Junnar,Dist.Pune-410511

JAIHIND COMPREHENSIVE EDUCATIONAL INSTITUTE'S
JAIHIND COLLEGE OF ENGINEERING, KURAN
Affiliated to Savitribai Phule Pune University
DTE :- EN6609 SPPU:- CEGP015730

Department of Electronics & Telecommunication Engineering

NOTICE **Date:22/02/2024**

All Students hereby informed that department of Electronics &Telecommunication, Engineering has arranged seminar on VLSI on Thursday,29/02/2024 so all students should attend the seminar compulsory.

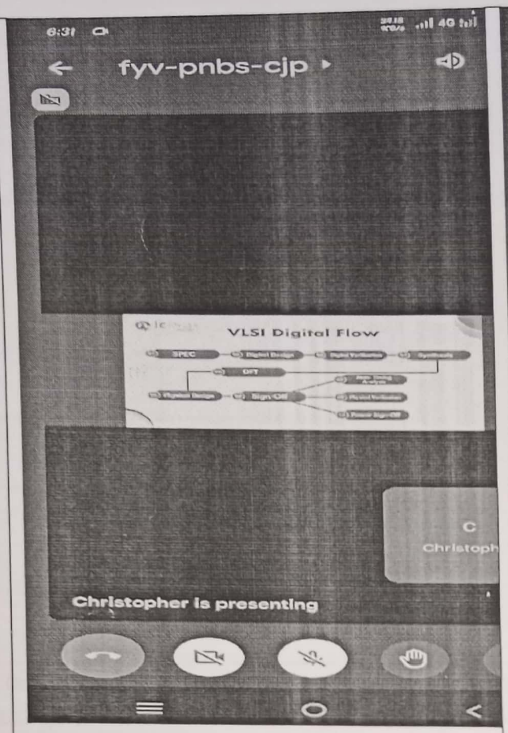
Event Co-Ordinator

HOD 22/02/24
Head of Department
(E & TC)
JSPM's Jaihind College of Engineering
Kuran, Tal-Junnar, Dist. Pune

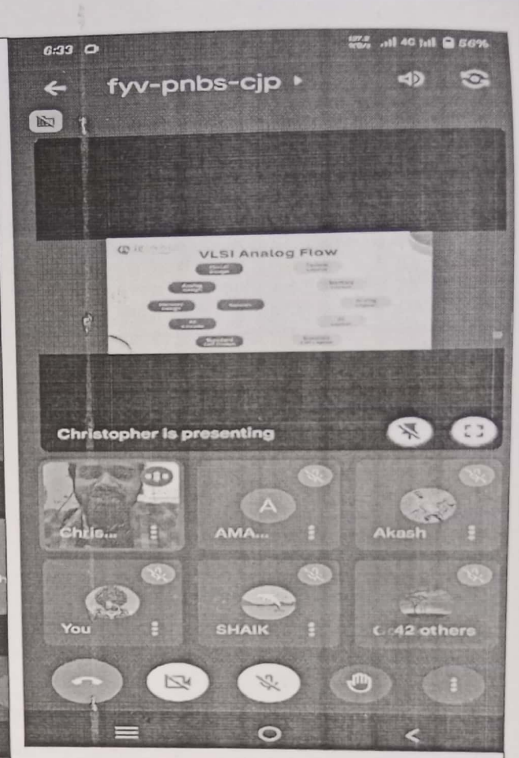
Activity Report

Organizing Department	*Electronics & Telecommunication Engineering*		
Name of The Event	*Seminar on VLSI*		
Date	*29 Feb 2024*		
Event location	*Online*		
Duration in Days/Hrs.	*01*		
Collaborative Agency / MoU / Organization	*Maven Silicon*		
Name of the Resource Person	*Christopher*		
Objectives	1. Importance of VLSI design in the current world scenario. 2. Solid introductory knowledge on VLSI concepts using standard introductory tools.		
a. No. of Students attendees	*b. No. of Faculty Attendees*	*c. No. of Other Attendees*	*Total attendance (a + b + c)*
74	*05*	-	*79*
Fund allocated By Institute	*Funding body (if any)*	*Total Expenditure in INR*	
JCOE	-	-	
Event Summary Report	The seminar on VLSI was organized and coordinated by the department of Electronics and Telecommunication Engineering of Jaihind College of Engineering, on Thursday, 29th April 2024, in the college premises. The Chief Guest & the expert key speaker of this event is Mr. Christopher. This seminar was conducted exclusively for pre-final year students and for Second, Third year students. The motive of the seminar was to improve the knowledge on VLSI for the students & provide instincts in the current technological trends in the field.		

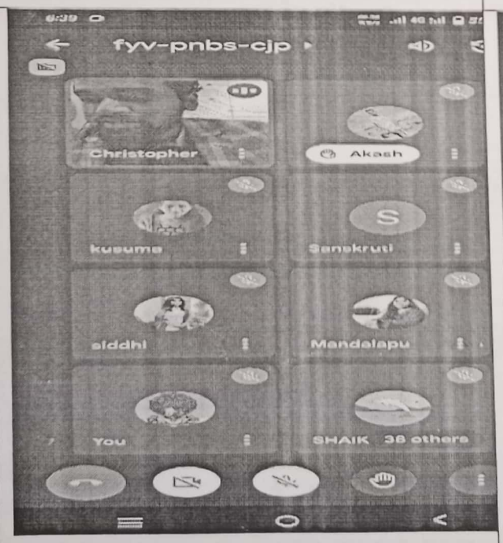
Event Photos



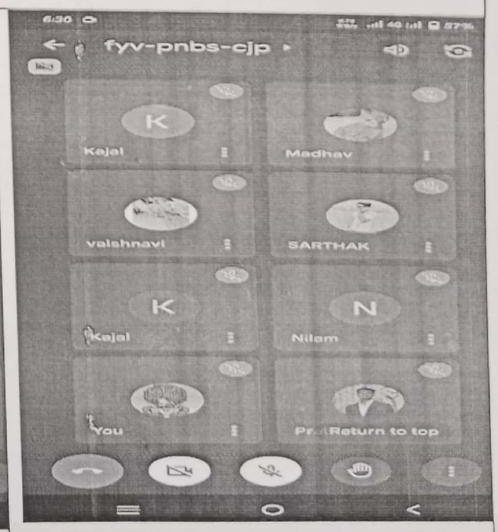
Introduction to VLSI



Current Flow of VLSI



Students attended Seminar



Question Answer Session

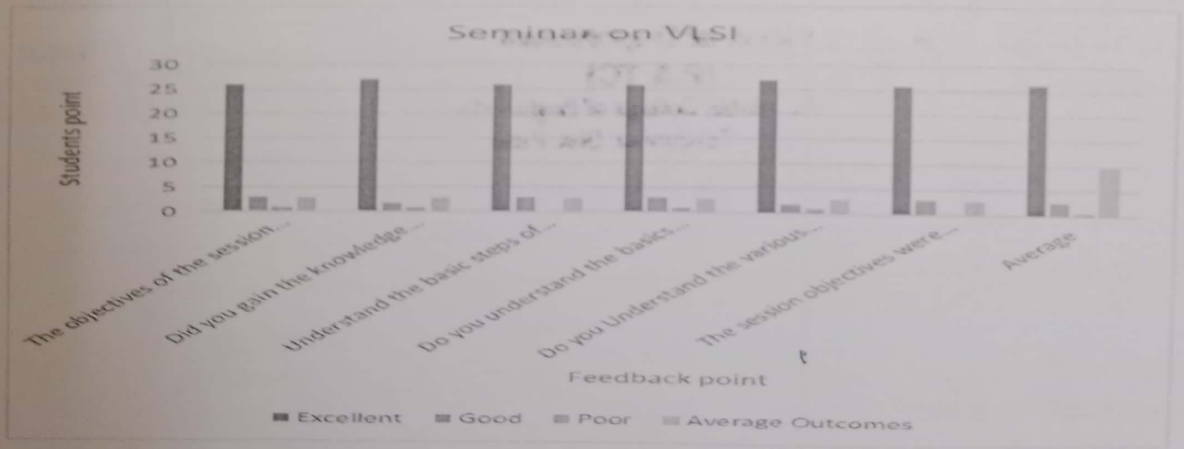
Feedback Analysis

Total Feedback Evaluated -30

No.	Sr. No	Question	Excellent (3)	Good (2)	Poor (1)	—
1	1	The objectives of the session were clearly defined.	26	3	1	2.83
	2	Did you gain the knowledge about the Features of VLSI?	27	2	1	2.86
	3	Understand the basic steps of fabrication	26	3	0	2.8
	4	Do you understand the basics of different processors including architecture and organization?	26	3	1	2.83
	5	Do you Understand the various advanced architectures?	27	2	1	2.86
	6	The session objectives were met?	26	3	0	2.8
		Average	26.33	2.66	0.66	9.88
2		Please rate the experience at the Guest/ Expert Lecture?	5			
3		Would you like to attend such more lectures in future?	Yes			

Remark-

Graphical Analysis



Event Outcomes (EO)-

1. Demonstrate the VLSI verification techniques.
2. Develop design using system Verilog.

EO-PO Mapping-

EO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EO1			2									
EO2		2										

Event Coordinator

Head of Department

Head of Department (E & TC)
JSPM's Jaihind College of Engineering
Tal-Junnar, Dist. Pune

IQAC

Director
Internal Quality Assurance Cell
Jaihind College of Engineering, Kuran
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Principal

Principal
JSPM's Jaihind College Of Engineering
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Department of Electronics and Telecommunication Engineering

ATTENDANCE LIST

A.Y.2023-24

Date-20/04/2024

Event Name – Guest lecture on Object Oriented Programming

SR.NO	Name	Year/Class	Sign
1)	Bhor Rutuja Bhausaheb	SE E&TC	Rutuja
2)	Benke Sakshi Sopan.	SE E&TC	Sbenake.
3)	Bhor Sawali Anil	S.E.	ABhor
4)	Chavan Shruti Baliram	S.E.	Chavan
5)	Lembhe Shruttka Sachin	SE E&TC	Aembhe
6.	Diksha vitthal Jedgwe	SEENTC	Dkanitkar
7.	Kanitkar Maunali Uday	SE	Mkanitkar
8.	Pokharkar Aditi Baban	SE	Pokharkar
9.	Durgude Sanika Mukund	SE.	Adurgude
10	Kumbhar Vaishnavi Devidas	SE	Vkumbhar
11.	Pansare Priyanka Sunil	S.E	Pansare
12.	Jadhav Aparna Vilas	S.E	
18.	Jadhav Apeksha Vilas	S.E	
14.	Dakh Akanksha Govindrao	SE	Dakh
15.	Panchal Aishwarya Yeknath	SE	Spanc
16	Shruti santosh Shirsath	SE	
17	Neharkar Ankita mahadev	SE	Aneharkar.
18	Dhamak Akanksha Ajit	SE	ADhamak
19	Shinde Vaishnavi Narendra	SE	V.Nshinde
20	Naykodi Sakshi Bhimaji	S.E	NaykodiSB
21	Khandagale Renuka Ashok	S.E	Aenuka
22	Mengade Shilpa Bhausaheb	S.E	Amengade
23	Sakshi Rajendra minde	SE	Sminde
24	Dhanashree Ankush Wagh	SE	Dwagh
25	Dokesarthak Narayan	S.E	Dake
26	Thorat Nikhil Ganpat	S.E	NTiwk

Coordinator

HOD
Head of Department
(E & TC)
JSPM's Jaihind College of Engineering
Kuran, Tal-Junnar, Dist. Pune

Certificates

iclabs

CERTIFICATE
OF PARTICIPATION

THE FOLLOWING AWARD IS GIVEN TO

Kajal Vijay Shete

expand their knowledge through this 2 hour VLSI Seminar.

Prasad Rallabandi
Founder and CEO

Rupa R
Director

iclabs

CERTIFICATE
OF PARTICIPATION

THE FOLLOWING AWARD IS GIVEN TO

Sonam Balasaheb Bangar

This certificate is given to Sonam Balasaheb Bangar for their dedication to acquire and expand their knowledge through this 2 hour VLSI Seminar.

Prasad Rallabandi
Founder and CEO

Rupa R
Director

iclabs

CERTIFICATE
OF PARTICIPATION

THE FOLLOWING AWARD IS GIVEN TO

SAWALI ANIL BHOR

This certificate is given to SAWALI ANIL BHOR for their dedication to acquire and expand their knowledge through this 2 hour VLSI Seminar.

Prasad Rallabandi
Founder and CEO

Rupa R
Director